ABSTRACT OF THE DISCLOSURE

Direct Memory Access Control

A direct memory access controller for controlling data transfer between a data source and a data destination comprising: a read/write port operable to receive data from said data source via a source bus and to output said received data to said data destination via a destination bus; wherein said direct memory access controller is operable in response to a predetermined number of clock pulses, to control said read/write port to output said received data said predetermined number of clock pulses after having received it. Also a direct memory access controller for controlling data transfer between a data source and a data destination comprising: a single read/write port comprising a read channel operable to receive data from said data source via a read path on a bus and a write channel operable to output said received data to said data destination via a write path on said bus, said read and write channel being operable to perform data reads and writes independently of each other.

Fig 5